2023-2024

Workshop

on

"Digital Logic Design"

By

Mr.K.Subash Chandra Naidu M.Sc, B.Ed

Lecturer
Department of Electronics,
St. Joseph's Degree College, KURNOOL.

Academic Year

2023-2024

Faculty Attended

Computer Science Department

Faculty members of various Degree Colleges,

Rayalaseema University, KURNOOL.

Course Co-ordinators:

Mr. K. Amarnath
Mr. A.Viswanatha Rao

Request Letter

05-02-2024,
Kurnool.

To
The Chairman,
Internal Quality Assurance Cell,
St. Joseph's Degree College,
Kurnool.

Respected Sir/Madam,

Sub: - Request for permission to conduct2-Day work shop- "Digital Logic Design" – Reg.

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Computer Science Department, St. Joseph's Degree College planning to organize a 2-Day workshop on "**Digital Logic Design**" by Mr. Subash Chandra Naidu, Lecturer, Department of Electronics, St. Jospeh's Degree College. Kurnool.

So, I request to consider the proposal and permit the department to organize 2-Day workshop.

With Regards,

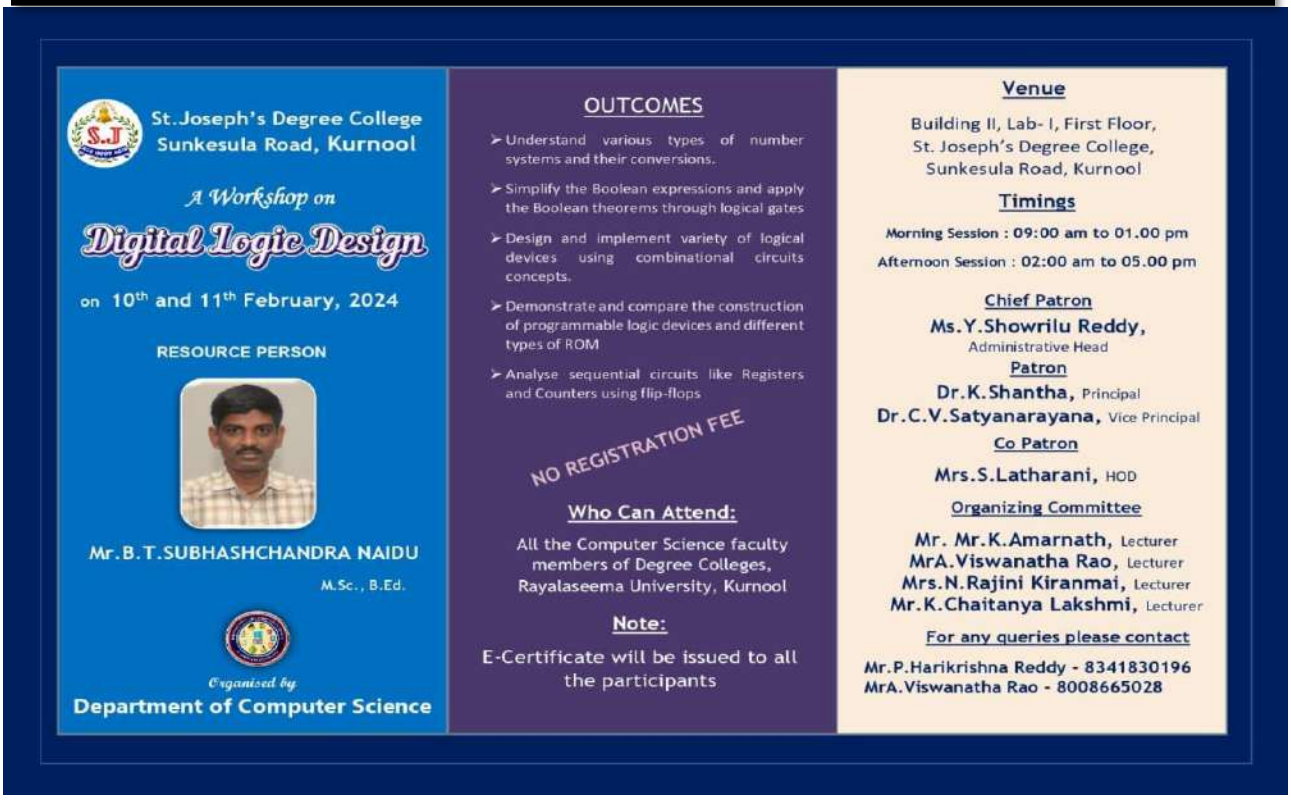
(S Latha Rani)
Head, Computer Science Department.

Copy to:

1. Copy to Principal

Brochure


St.Joseph's Degree College
Sunkesula Road, Kurnool.
Department of Computer Science
Welcome
To
Workshop on
Digital Logic Design
Resource Person
Mr. B.T.Subhash Chandra Naidu
M.Sc., B.Ed.
Organization Committee
Mr. K.Amarnath, Lecturer.
Mr. A.Viswanatha Rao, Lecturer.
Mrs. N. Rajini Kiranmai, Lecturer.
Mrs. K.Chaitanya Lakshmi, Lecturer.
Chief Patron
Ms. Y.Showrilu Reddy,
Administrative Head.
Patron
Dr. K. Shantha, Principal.
Dr. C.V. Satyanarayana,
Vice-Principal.
Date: 10th and 11th
Feb - 2023
Co-Patron
Mrs. S.Latha Rani, HOD


St.Joseph's Degree College
Sunkesula Road, Kurnool
A Workshop on
Digital Logic Design
on 10th and 11th February, 2024
RESOURCE PERSON
Mr.B.T.SUBHASHCHANDRA NAIDU
M.Sc., B.Ed.
Organised by
Department of Computer Science
OUTCOMES
Understand various types of number systems and their conversions.
Simplify the Boolean expressions and apply the Boolean theorems through logical gates
Design and implement variety of logical devices using combinational circuits concepts.
Demonstrate and compare the construction of programmable logic devices and different types of ROM
Analyse sequential circuits like Registers and Counters using flip-flops
NO REGISTRATION FEE
Who Can Attend:
All the Computer Science faculty members of Degree Colleges, Rayalaseema University, Kurnool
Note:
E-Certificate will be issued to all the participants
Venue
Building II, Lab- I, First Floor,
St. Joseph's Degree College,
Sunkesula Road, Kurnool
Timings
Morning Session : 09:00 am to 01.00 pm
Afternoon Session : 02:00 am to 05.00 pm
Chief Patron
Ms.Y.Showrilu Reddy,
Administrative Head
Patron
Dr.K.Shantha, Principal
Dr.C.V.Satyanarayana, Vice Principal
Co Patron
Mrs.S.Latharani, HOD
Organizing Committee
Mr. Mr.K.Amarnath, Lecturer
MrA.Viswanatha Rao, Lecturer
Mrs.N.Rajini Kiranmai, Lecturer
Mr.K.Chaitanya Lakshmi, Lecturer
For any queries please contact
Mr.P.Harikrishna Reddy - 8341830196
MrA.Viswanatha Rao - 8008665028

2-Days Work Shop on Digital Logic Design

Work shop is a powerful peer assessment activity to discuss and perform practical work in a subject or an activity. It is structured and interactive session designed to create an environment for meaningful work and to guide a group through a process that will lead to great outcomes.

Computer Science Department organized a 2-Day workshop on Digital Logic Design in order to enhance, engage the faculty to foster their ability in DLD.

Mr. K.Subash Chandra Naidu,Lecture,Kurnool was the right person to do so. The main objective of the workshop is to learn DLD practically using electronic equipment as DLD got introduced in curriculum for this academic year.

Dates: 10^{th},11^{th} Feb 2024.

Time: 9am – 5pm.

Place: Lab2, Building 2, St.Joseph's Degree College.

Topic:Digital Logic design

Resource person: Mr. K.SubashChandra Naidu,

Designation: Lecturer, Department of Electronics, St. Jospeh's Degree College. Kurnool.

Outcomes of the workshop:

- To various types of number systems and their conversions.
- To simplify the Boolean expression and apply the Boolean theorems through logical gates.
- To design and implement variety of logical devices using combinational circuits concepts.
- To Demonstrate and compare the construction of programmable logic devices and different types of ROM.
- To analyze sequential circuits like Registers and counters using flip-flops.

II Semester

Course 4: Digital Logic Design

Credits -3

Course Objectives

To familiarize with the concepts of designing digital circuits.

Course Outcomes

Upon successful completion of the course, the students will be able to

1. Understand how to Convert numbers from one radix to another radix and performarithmetic operations.
2. Simplify Boolean functions using Boolean algebra and k- maps
3. Design adders and subtractors circuits
4. Design combinational logic circuits such as decoders, encoders, multiplexers and demultiplexers.
5. Use flip flops to design registers and counters.

UNIT – I

Number Systems: Binary, octal, decimal, hexadecimal number systems, conversion of numbers from one radix to another radix, r's, (r-1)'s complements, signed binary numbers, addition and subtraction of unsigned and signed numbers, weighted and unweighted codes.

UNIT – II

Logic Gates and Boolean Algebra: NOT, AND, OR, universal gates, X-OR and X-NOR gates, Boolean laws and theorems, complement and dual of a logic function, canonical and standard forms, two level realization of logic functions using universal gates, minimizations of logic functions (POS and SOP) using Boolean theorems, K-map (up to four variables), don't care conditions.

UNIT – III

Combinational Logic Circuits – 1: Design of half adder, full adder, half subtractor, fullsubtractor, ripple adders and subtractors, ripple adder / subtractor.

UNIT – IV

Combinational Logic Circuits – 2: Design of decoders, encoders, priority encoder, multiplexers, demultiplexers, higher order decoders, demultiplexers and multiplexers, realization of Boolean functions using decoders, multiplexers.

UNIT – V

Sequential Logic Circuits: Classification of sequential circuits, latch and flip-flop, RS- latch using NAND and NOR Gates, truth tables, RS, JK, T and D flip-flops, truth and excitation tables, conversion of flip- flops, flip-flops with asynchronous inputs (preset and clear).

Design of registers, shift registers, bidirectional shift registers, universal shift register, design of ripple counters, synchronous counters and variable modulus counters.

Text Books:

Agenda

Objectives of The Workshop:

- To familiarize with the concepts of designing digital circuits.
- To acquire the basic knowledge of digital logic levels and application of knowledge to understand digital electronics circuits.
- To prepare participants to perform the analysis and design of various digital electronic circuits.

Expected Outcomes:

After this workshop, the participants would gain enough knowledge

- Have a thorough understanding of the fundamental concepts and techniques used in digital electronics.
- To understand and examine the structure of various number systems and its application in digital design.
- The ability to understand, analyze and design various combinational and sequential circuits.
- The ability to identify and prevent various hazards and timing problems in a digital design.
- To develop skill to build, and troubleshoot digital circuits.

Program – Day- I:

Time	**Activity**	**Remarks**
08.45 am	Arrival of participants	
9.00 am to 9.30 am	Inviting guests on to the Dias	
	Prayer Song	
	Welcome Note and presentation of workshop program and objectives	By Mr. **K.Amarnath**
	Opening Remarks	By **Mrs.S.Latha Rani, HOD**
	Address by Vice Principal Dr.**C.V.Satyanarayana**	
	Address by Principal Dr. **K.Shantha**	
09:30 am to 11.00 am	Session – I	
11.00 am to 11.15 am	**Tea Break**	
11.15 am to 1.00 pm	Session –II	
1:00 pm to 2:00 pm	**Lunch Break**	
2.00 pm to 3:30 pm	Session –III	Demo of Practical implementation
3.30 pm to 3.45 pm	**Tea Break**	
3.45 pm to 5.00 pm	Session – IV & End of Day – I	Practical implementation by participants

Program – Day – II :

Time	Activity	Remarks
09:00 am to 11.00 am	Session – I	
11.00 am to 11.15 am	***Tea Break***	
11.15 am to 1.00 pm	Session –II	Practical implementation by Participants
1:00 pm to2:00 pm	**Lunch Break**	
2.00 pm to 4.00 pm	Valedictory & closing ceremony	

Syllabus

Day 1:

Morning Session :

- Signed binary numbers, addition and subtraction of unsigned and signed numbers.
- Weighted and unweighted codes.
- NOT, AND, OR, universal gates, X-OR and X-NOR gates.
- Boolean laws and theorems, complement and dual of a logic function.
- Canonical and standard forms.

Afternoon Session :
Practicals :

- Introduction to Electronic breadboard , Integrated Circuits (Logic gates) like AND, OR NOT,XOR .
- PIN configuration of logic gates. Testing of basic Logic gates.

Day 2:

Morning Sessin :

- Two level realization of logic functions using universal gates.
- Minimizations of logic functions (POS and SOP) using Boolean theorems.
- K-map (up to four variables).
- Don't care conditions..

Afternoon Session :

Practicals :

- Design of half adder and Half subtractor

Attendance Sheets

St.Joseph's Degree College, Sunkesula Road, Kurnool

Workshop on "Digital Logic Design" 10th & 11th February , 2024

Online Attended Participants Details

Sno	Name of the Faculty	College	Mobile	Email Id
1	S BhaskaraNaik	SVB Govt Degrees college	8309827895	baskarnaik808@gmail.com
2	Dr M SreeDevi Associate professor Sv University Tirupati	Sv University , Tirupati	8309827895	baskarnaik808@gmail.com
3	SHAIK NAFIYA	Government Degree College, Atmakur	6281364406	nafiyasnr@gmail.com
4	Boya Hussain	Dr.jothirmy Degeree college adoni	8184855847	hussain.boya@gmail.com
5	Emmiganur Lakshmi Kantha gouda	SSAGovt Degree,college -Ballari	9620177901	kantha816@gmail.com
6	Syed Fairoz Ahmed	Vasavi Mahila Kalasala	9963037238	fairoz_ahmed1983@yahoo.com
7	D.PULLAIAH	Kvsr degree college.Allagadda	7893382336	pullaiah786@gmail.com
8	P KRISHNA KISHORE REDDY	PRAGNA DEGREE COLLEGE	7093799698	Palle.kkreddy1983@gmail.com
9	K Sampath Kumar	Sri Ravi Degree College	9989003313	Ksksarma@gmail.com
10	C. Naga Pradeep Kumar	SML Government Degree College	9949481581	nagapradeep.srit@gmail.com
11	K Manoranjan Kumar	SML GDC Yemmiganur	9949426246	manoranjan9949@gmail.com
12	Dupati Swetha	R. C. Reddy Degree College	9573738237	dupati.swetha2@gmail.com
13	C BADULLA	National Degree College Nandyal	9885619553	badullamsc@gmail.com
14	M. MALATHI	Ravindra degree college for women	9703062465	malathi.keerthan@gmail.com
15	MAHAMMAD RAFI. B	NATIONAL DEGREE COLLEGE, NANDYAL	9866449900	rafimail73@gmail.com
16	SAIQUA ZAREEN	St.Joseph's Degree College	9030917408	saiquaaisha13@gmail.com
17	Madduri Joyce	St Joseph's Degree College	9951741678	joycemadduri1234@gmail.com
18	K.Vanitha kumari	St Joseph's degree college kurnool	7306565096	kesanavanitha@gmail.com
19	SHAIK MOHAMMED ZAHEERUDDIN	GDC. NANDYAL	7386555596	zaheermohammedd@gmail.com
20	S AFSHAN ANJUM	St Joseph's Degree College	9032147921	shaikafshanjum@gmail.com
21	T. Sreelakshmi	Sri Sai Krishna degree college	9885493434	thotasreelakshmikni@gmail.com
22	T ADINARAYANA	S N S R DEGREE COLLEGE VELGODE	9492942060	adhinarayana010@gmail.com
23	M.Usha	Vyshnavi Degree College, Yemmiganur	9705975815	ushasri196@gmail.com
24	Dr.M.Balasubramanyam	SRI RAMAKRISHNA DEGREE COLLEGE NANDYAL	6304030063	mbalasubramanyam4@gmail.com

Head
Dept. of Comp. Science
St Joseph's Degree College
KURNOOL

St.Joseph's Degree College, Sunkesula Road, Kurnool

Workshop on "Digital Logic Design"

Attendance Sheet

Sno	Name	College	Place	Day 1 10-Feb-2024		Day 2 11-Feb-2024	
				FN	AN	FN	AN
1	P Sai Srujana	St.Joseph's Degree College	Kurnool				
2	P. Armila Devi	St.Joseph's Degree College	Kurnool				
3	D Mahaboob Basha	Sri Saikrishna Degree College	Kurnool				
4	I S Raghuram	St.Joseph's Degree College	Kurnool				
5	B. Manju Bhargavi	St.Joseph's Degree College	Kurnool				
6	Raghavendra Kumar V	St.Joseph's Degree College	Kurnool				
7	A. Viswanatha Rao	St.Joseph's Degree College	Kurnool				
8	J.Rajaratnam	St.Joseph's Degree College	Kurnool				
9	J.Ramesh	St.Joseph's Degree College	Kurnool				
10	G.P.Babu	St.Joseph's Degree College	Kurnool				
11	N.Rajini Kiranmai	St.Joseph's Degree College	Kurnool				
12	K.Chaitanya Lakshmi	St.Joseph's Degree College	Kurnool				
13	P.Harikrishna Reddy	St.Joseph's Degree College	Kurnool				
14	O.Kiran Kumar	St.Joseph's Degree College	Kurnool				
15	A.Mallikarjuna	St.Joseph's Degree College	Kurnool				
16	K.Amarnath	St.Joseph's Degree College	Kurnool				
17	S.Latha Rani	St.Joseph's Degree College	Kurnool				
18	S.Jahara Bi	Sri Sankara's Degree College	Kurnool				
19	S.Bhaskar Rao	Sri Vivekananda Degree College	Kodumur				

Head
Dept. of Comp. Science
St Joseph's Degree College
KURNOOL

Feedback

- Faculty members of Computer Science Departments, Rayalaseema University Affiliated Colleges.
- TotalNo.ofParticipantsRegistered: **43**
- TotalNo.ofParticipants Attended: **43**

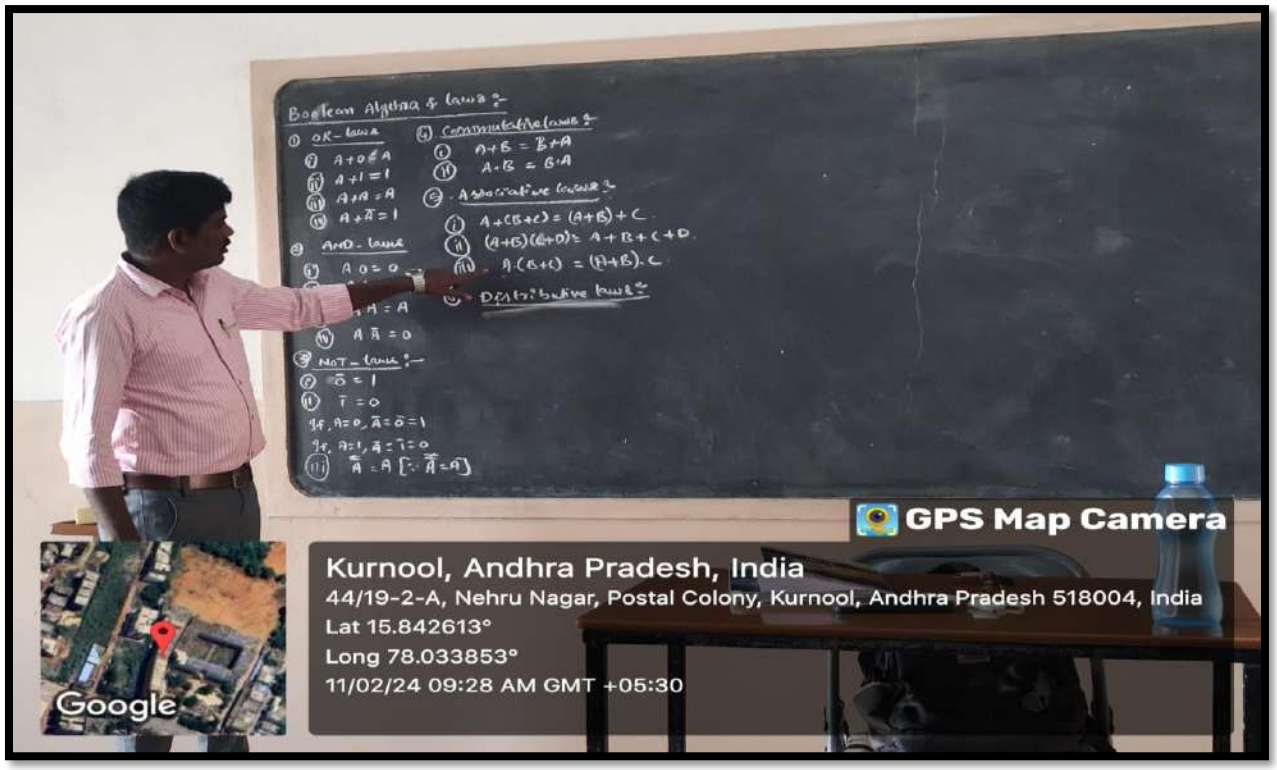
GoogleDriveLinkforRegistrationforms:

https://forms.gle/6ZRSwAueXQWNzgfX8

GoogleDriveLinkforFeedback forms:

https://forms.gle/AEoSAJucfKEya7NT8

2-Day work shop - PHOTOS




GPS Map Camera
Kurnool, Andhra Pradesh, India
44/19-2-A, Nehru Nagar, Postal Colony, Kurnool, Andhra Pradesh 518004, India
Lat 15.842603°
Long 78.033895°
11/02/24 12:28 PM GMT +05:30
Google

Sample Certificate

St. Joseph's Degree College

Sunkesula Road, Kurnool

CERTIFICATE

Of Partificipation

This Certificate is Presented to

Mr./Mrs. D MAHABOOB BASHA of

SRI SAIKRISHNA DEGREE COLLEGE, KURNOOL

for participating in a Workshop on

DIGITAL LOGIC DESIGN

in 10th & 11th February, 2024

Organized by **Department of Computer Science**

S.Latha Rani
HOD
Dept. of Computer Science

Dr. C.V. Satyanarayana
Vice Principal

Dr.K.Shantha
Principal